

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Kun-Lin WU, et al

Serial No. Unassigned

Filed: November 20, 2001

For: CHEMICAL-MECHANICAL
POLISHING METHOD

Examiner: Unassigned

Art Unit: Unassigned

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
2900 Crystal Drive
Arlington, VA 22202-3513

Sir:

Please amend the copy of U.S. Patent Application Serial No.
09/563,030, filed herewith, as follows:

IN THE SPECIFICATION

On page 1, lines 5–7, please amend the specification as follows:

[This application claims the priority of Taiwan application serial no. 87110514, filed June 30, 1998, the full disclosure of which is incorporated herein by reference.] The present application is a continuation of co-pending U.S. Patent Application Serial No. 09/563,030, filed May 1, 2000, which is a continuation of U.S. Patent Application Serial No. 09/132,876, filed August 11, 1998, now U.S. Patent No. 6,077,784, which claims priority from Taiwan Application No. 87110514, filed June 30, 1998, all the disclosures of which are herein specifically incorporated by this reference.

IN THE CLAIMS

Please cancel claims 1–27.

Please add claims 28–44 according to the attached sheets.

REMARKS

The amendment adds new claims 28–44 while canceling claims 1–27, making claims 28–44 pending in the application. Support for the amendment can be found in the parent application and patent. No new matter has been added by the amendment.


William J. Kubida, et al (Customer No. 25235) was appointed the attorney of record in this case in a power of attorney filed October 11, 2001 (a copy of which is included herewith). Please confirm that correspondence in this case should be directed to:

William J. Kubida, Reg. No. 29,664
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The entry of this Amendment and advancement of the application to allowance is respectfully requested. If the Examiner has any questions, she or he is requested to contact the undersigned at the telephone listed below.

Respectfully submitted,

November 20, 2001


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CLEAN VERSION OF THE AMENDMENT

IN THE SPECIFICATION

The present application is a continuation of co-pending U.S. Patent Application Serial No. 09/563,030, filed May 1, 2000, which is a continuation of U.S. Patent Application Serial No. 09/132,876, filed August 11, 1998, now U.S. Patent No. 6,077,784, which claims priority from Taiwan Application No. 87110514, filed June 30, 1998, all the disclosures of which are herein specifically incorporated by this reference.

IN THE CLAIMS

28. (New) A chemical-mechanical polishing process, comprising the steps of:

forming a first conductive layer and a dielectric layer over a semiconductor substrate;
polishing the dielectric layer to form a substantially planar surface; and
forming a dielectric cap layer over the dielectric layer.

29. (New) The process of claim 28, wherein the step of forming the conductive layer includes depositing doped polysilicon.

30. (New) The process of claim 28, wherein the step of forming the dielectric layer includes a high-density plasma chemical vapor deposition method.

31. (New) The process of claim 28, wherein the step of forming the dielectric layer includes depositing silicon dioxide.

32. (New) The process of claim 28, wherein the step of forming the dielectric layer includes depositing silicon dioxide.

33. (New) The process of claim 28, wherein the step of forming the cap layer includes depositing a silicon oxide layer using a plasma-enhanced chemical vapor deposition method with silane (SiH_4) as the main reactive agent.

34. (New) The process of claim 28, wherein the silicon oxide layer is deposited to a thickness of about 1000-3000 Angstroms and can be adjusted according to design rules.

35. (New) The process of claim 28, wherein the step of forming the cap layer includes depositing a silicon oxide layer using a chemical vapor deposition method with tetra-ethyl-ortho-silicate (TEOS) as the main reactive agent.

36. (New) The process of claim 28, wherein the silicon oxide layer is deposited to a thickness of about 1000-3000 Angstroms and can be adjusted according to design rules.

37. (New) The process of claim 28, wherein the step of forming the cap layer includes depositing a silicon nitride layer using a chemical vapor deposition method with silane (SiH_4) as the main reactive agent.

38. (New) The process of claim 28, wherein the silicon nitride layer is deposited to a thickness of about 100-3000 Angstroms and can be adjusted according to design rules.

39. (New) The process of claim 28, wherein the step of forming the cap layer includes depositing a silicon nitride layer using a chemical vapor deposition method with silicon dichlorohydride (SiH_2Cl_2) as the main reactive agent.

40. (New) The process of claim 28, wherein the silicon nitride layer is deposited to a thickness of about 100-3000 Angstroms and can be adjusted according to design rules.

41. (New) The process of claim 28, wherein the step of forming the cap layer includes depositing silicon dioxide.

42. (New) The process of claim 28, wherein the step of forming the cap layer includes depositing phosphosilicate glass (PSG).

43. (New) The process of claim 28, wherein the step of forming the cap layer includes depositing silicon-rich oxide (SRO).

44. (New) A process of forming a conductive interconnect, the process comprising the steps of:

providing a semiconductor substrate having a conductive layer thereon;

forming a dielectric layer over the substrate and the conductive layer;

polishing the surface of the dielectric layer to form a substantially planar surface; and

forming a dielectric cap layer over the dielectric layer.